

1 CLAIMS:

2 1. An integrated circuit device comprising:

3 a semiconductor die;

4 a first housing encapsulating the semiconductor die;

5 a heat sink positioned proximate to the first housing; and

6 a second housing encapsulating at least a portion of the heat
7 sink.

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9 2. The integrated circuit device according to claim 1 further
10 comprising at least one first lead coupled with the semiconductor die
11 and the first housing encapsulates at least a portion of the at least one
12 first lead.

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14 3. The integrated circuit device according to claim 1 wherein
15 the heat sink comprises:

16 a body; and

17 at least one second lead coupled with the body and the second
18 housing encapsulates at least a portion of the at least one second lead.

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20 4. The integrated circuit device according to claim 3 wherein
21 the at least one second lead is configured to dissipate heat from the
22 semiconductor die.

1 5. The integrated circuit device according to claim 1 wherein
2 the second housing encapsulates a majority of the heat sink.
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4 6. The integrated circuit device according to claim 1 wherein
5 the second housing encapsulates a majority of the heat sink and at
6 least a portion of the first housing.
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8 7. The integrated circuit device according to claim 1 wherein
9 the second housing encapsulates a majority of the heat sink and a
10 majority of the first housing.
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12 8. The integrated circuit device according to claim 1 wherein
13 the semiconductor die comprises a synchronous-link dynamic random
14 access memory device and the second housing forms one of a vertical
15 surface mounted package and a horizontal surface mounted package.
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1 9. An integrated circuit device comprising:
2 a semiconductor die having a plurality of bond pads;
3 a plurality of leads electrically coupled with the bond pads of the
4 semiconductor die;
5 a first housing encapsulating the semiconductor die and at least
6 a portion of the leads;
7 a heat sink thermally coupled with the first housing; and
8 a second housing encapsulating at least a portion of the heat
9 sink.

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11 10. The integrated circuit device according to claim 9 wherein
12 the heat sink comprises a metal and the first housing contacts the
13 metal.

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15 11. The integrated circuit device according to claim 9 wherein
16 the heat sink includes at least one lead configured to dissipate heat
17 from the semiconductor die.

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19 12. The integrated circuit device according to claim 9 wherein
20 the second housing forms one of a vertical surface mounted package
21 and a horizontal surface mounted package.

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23 13. The integrated circuit device according to claim 9 wherein
24 the second housing encapsulates the first housing.

1 14. An integrated circuit device comprising:
2 a first housing formed about a semiconductor die and at least
3 portions of a plurality of leads electrically coupled with the
4 semiconductor die;

5 a heat sink thermally coupled with the first housing; and
6 a second housing formed about the heat sink and at least a
7 portion of the first housing.

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9 15. The integrated circuit device according to claim 14 wherein
10 the first housing and second housing individually comprise an
11 encapsulant housing.

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13 16. The integrated circuit device according to claim 14 wherein
14 the heat sink contacts the first housing.

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16 17. The integrated circuit device according to claim 14 wherein
17 the heat sink further includes at least one lead configured to dissipate
18 heat from the semiconductor die.

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1 18. A synchronous-link dynamic random access memory device
2 comprising:

3 a semiconductor die bearing synchronous-link dynamic random
4 access memory circuitry and having a plurality of bond pads coupled
5 therewith;

6 a plurality of leads electrically coupled with the bond pads of the
7 semiconductor die;

8 a first housing encapsulating the semiconductor die and at least
9 a portion of the leads;

10 a heat sink positioned proximate the first housing and configured
11 to draw heat from the semiconductor die; and

12 a second housing encapsulating the heat sink and at least a
13 portion of the first housing.
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15 19. The synchronous-link dynamic random access memory device
16 according to claim 18 wherein the second housing forms one of a
17 vertical surface mounted package and a horizontal surface mounted
18 package.
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20 20. The synchronous-link dynamic random access memory device
21 according to claim 18 wherein the heat sink comprises at least one lead
22 configured to dissipate heat from the semiconductor die.
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1 21. A method of forming an integrated circuit device comprising:
2 providing a semiconductor die;
3 forming a first housing about the semiconductor die;
4 thermally coupling a heat sink with the first housing; and
5 forming a second housing about at least a portion of the heat
6 sink following the thermally coupling.

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8 22. The method according to claim 21 wherein the providing
9 comprises providing a semiconductor die coupled with plural leads of a
10 lead frame.

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12 23. The method according to claim 22 further comprising
13 bending the leads to form one of a vertical surface mounted package
14 and a horizontal surface mounted package.

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16 24. The method according to claim 21 wherein the forming the
17 first housing and the forming the second housing individually comprise
18 encapsulating.

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20 25. The method according to claim 21 wherein the forming the
21 second housing comprises encapsulating at least a portion of the first
22 housing.

1 26. The method according to claim 21 further comprising
2 providing the heat sink with at least one lead.
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4 27. A method of forming an integrated circuit device comprising:
5 providing a semiconductor die having a plurality of bond pads;
6 providing a first lead frame having a plurality of leads;
7 providing a second lead frame having a heat sink;
8 electrically coupling the bond pads of the semiconductor die with
9 the leads of the first lead frame;

10 first encapsulating the semiconductor die and at least a portion
11 of the leads, the first encapsulating forming a first housing;

12 thermally coupling the heat sink with the first housing; and

13 second encapsulating at least a portion of the heat sink forming
14 a second housing following the thermally coupling.
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16 28. The method according to claim 27 wherein the second
17 encapsulating further comprises encapsulating at least a portion of the
18 first housing.
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20 29. The method according to claim 27 wherein the second
21 encapsulating further comprises encapsulating a majority of the heat sink
22 and a majority of the first housing.
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1 30. The method according to claim 27 wherein the thermally
2 coupling comprises positioning the heat sink to contact the first housing.
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4 31. The method according to claim 27 further comprising
5 bending the leads to form one of a vertical surface mounted package
6 and a horizontal surface mounted package.
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8 32. The method according to claim 27 wherein the providing the
9 second lead frame comprises providing the heat sink with at least one
10 lead.
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12 33. A method of forming an integrated circuit device comprising:
13 providing a semiconductor die electrically coupled with a plurality
14 of leads;
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16 forming a first housing about the semiconductor die and at least
17 a portion of the leads;
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19 providing a heat sink; and
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21 forming a second housing about at least a portion of the heat
22 sink, the forming the second housing thermally coupling the heat sink
23 with the semiconductor die.
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25 34. The method according to claim 33 further comprising
26 positioning a heat sink proximate the first housing prior to forming the
27 second housing.
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1 35. The method according to claim 33 wherein the forming the
2 first housing and the forming the second housing individually comprise
3 encapsulating.

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5 36. The method according to claim 33 wherein the forming the
6 second housing comprises forming the second housing about at least a
7 portion of the first housing.

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9 37. The method according to claim 33 wherein the forming the
10 second housing comprises encapsulating at least a portion of the heat
11 sink and at least a portion of the first housing.

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13 38. The method according to claim 33 wherein the providing the
14 heat sink comprises providing the heat sink having at least one lead.

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16 39. The method according to claim 33 further comprising
17 bending the leads to form one of a vertical surface mounted package
18 and a horizontal surface mounted package.

1 40. A method of forming a synchronous-link dynamic random
2 access memory edge-mounted device comprising:
3 providing a semiconductor die having a plurality of bond pads;
4 providing a first lead frame having a plurality of leads;
5 providing a second lead frame having a heat sink;
6 electrically coupling the bond pads of the semiconductor die with
7 the leads of the first lead frame;
8 positioning the semiconductor die and the first lead frame within
9 a first mold following the electrically coupling;
10 first encapsulating the semiconductor die and at least a portion
11 of the leads within the first mold using a first encapsulant;
12 curing the first encapsulant forming a first housing;
13 removing the first housing from the first lead frame;
14 positioning the heat sink of the second lead frame to contact a
15 surface of the first housing;
16 providing the semiconductor die and the second lead frame within
17 a second mold following the positioning the heat sink;
18 second encapsulating the first housing and the heat sink within the
19 second mold using a second encapsulant;
20 curing the second encapsulant forming a second housing;
21 removing the second housing from the second lead frame;
22 trimming the leads; and
23 bending the leads to form one of a vertical surface mounted
24 package and a horizontal surface mounted package.